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Mfr. of low leakage poly:silicon thin-film transistor - including depositing thin alkali-resistant inorganic film on glass substrate before first silicon oxide layer

C92-037806 R(DE FR GB IT NL)

Low leakage current thin-film transistor is mfd. by: depositing a thin layer of alkali-inert material (2) on a glass substrate (1) of annealing pt. below 650°C; adding a thick CVD SiO_2 layer (3); adding a thin amorphous Si layer at 520-570°C; annealing at below 650°C in N_2 to form a large grain poly Si layer; patterning the poly Si to form islands; oxidising the islands at below 650°C to form thin gate oxide (6); adding a thick, heavily doped poly Si gate layer (8); lightly implanting source and drain areas (9,10); adding thin overall CVD SiO_2 (11); heavily doping poly Si (12, 13) adjacent the lightly doped source and drain; annealing at below 650°C; and hydrogenating at 200-400°C in an H_2 plasma.

ADVANTAGE

Transistors having low leakage current are formed on low-cost commercial glass substrates.

L(4-C2A, 4-C3, 4-C10B, 4-C12C, 4-C16, 4-E1)

PREFERRED

Inorganic layer (2) is 800-1200 Angstrom Si_3N_4. The glass substrate has an annealing pt. of 550-650°C. The thick poly Si layer is annealed at 580-620°C. The gate oxide (6) is formed at 550-650°C at 5-50 atmos. pressure.

The first and second layers have thicknesses respectively of 500-1500 and 4000-7000 Angstrom. The second poly Si layer is doped with BF_3.

MODIFIED METHOD (Claimed)

The thick SiO_2 layer (3) is deposited direct onto a semiconductor substrate, with the inorganic (nitride) layer (2) omitted.(10pp1550KGDwgNo1c/2).

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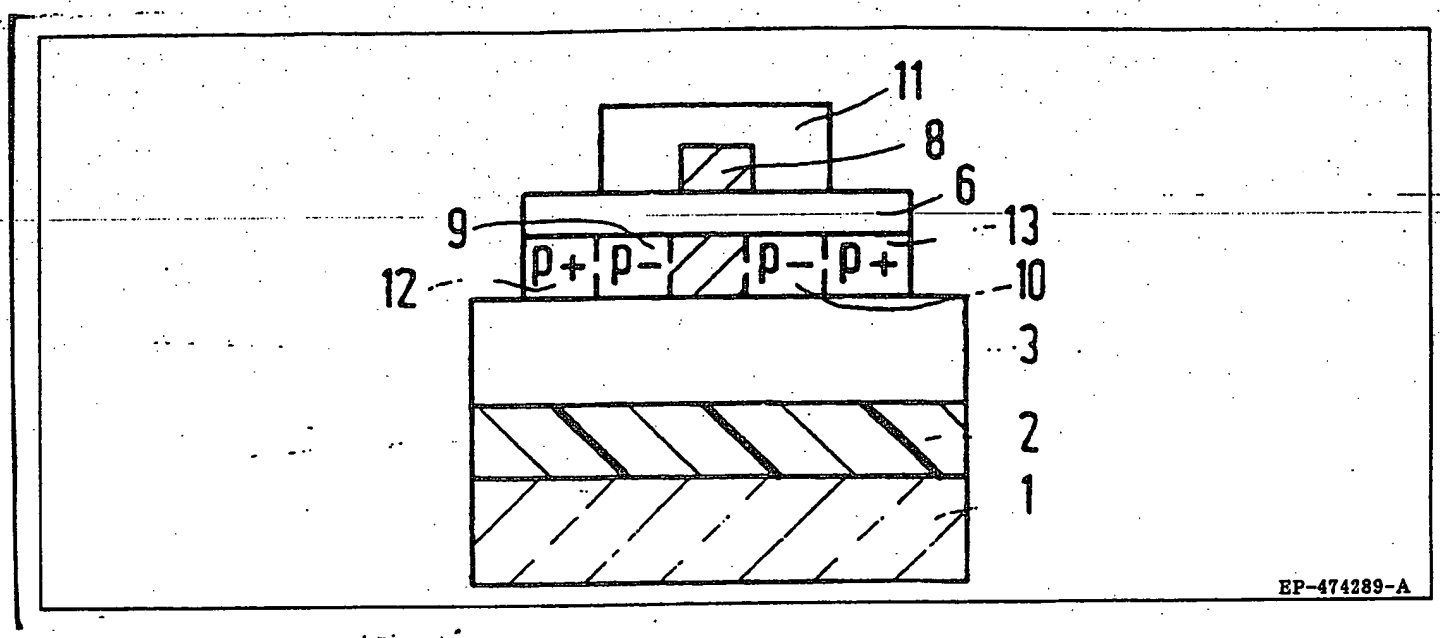

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(54) A method for the fabrication of low leakage polysilicon thin film transistors.

(57) According to one aspect of the invention thin film transistors exhibiting a reduced reverse leakage current are manufactured according to a method which includes the following steps:

Depositing a relatively thick layer of silicon oxide on a substrate by chemical vapor deposition, depositing a relatively thin polysilicon layer, annealing the relatively thin polysilicon layer at a temperature of less than 650 °C in a nitrogen atmosphere to cause large grain formation, forming islands by etching the thin polysilicon layer, forming a thin gate oxide layer on at least one of the islands by oxidation under high pressure at a temperature below 650 °C, depositing a relatively thick doped polysilicon layer on the gate oxide layer, forming a gate from the, relatively heavily doped, relatively thick polysilicon layer while having exposed laterally adjacent areas of the gate oxide layer and the underlying polysilicon island, lightly doping portions of the resultant exposed areas of the island of polysilicon laterally adjacent to the gate to form lightly doped source and drain areas, depositing a thin layer of silicon oxide on the gate and lightly doped source and drain areas, relatively heavily doping exposed areas of the layer of polysilicon laterally adjacent to the lightly doped source and drain areas to form relatively heavily doped source and drain areas, annealing the source and drain areas at a temperature of 600 °C to 750 °C and then hydrogenating the resultant device at a temperature of less than about a 400 °C with the hydrogen plasma.

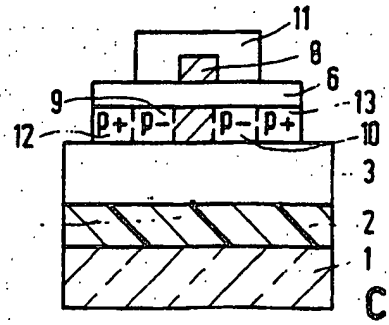

FIG.1

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employed: a thin layer of an alkali-inert inorganic material is deposited on the glass substrate prior to the depositing of the first relatively thick layer of silicon oxide. This additional step is carried out at a temperature of less than 650 ° C.

Figs. 1a, 1b and 1c of the drawing are views in section, and not in scale, of several stages employed in the production of a thin film transistor according to the method of the invention. Fig. 2 is a graph showing the relationship between gate voltage and drain or leakage current of a thin film transistor of the invention.

When the substrate is glass, preferably it is one having an annealing point of greater than 650 ° C. However, other glass substrates may be employed.

Preferably, the method of the invention for manufacturing a thin film transistor employing a glass substrate embodies first depositing a thin layer of an alkali inert inorganic material on a glass substrate. This alkali inorganic material may, for example, be silicon nitride. However other alkali-inert inorganic materials may be employed such as silicon oxynitrides. The thickness of the layer of the alkali-inert inorganic material preferably is about 800-1200 Å. A relatively thick layer of silicon oxide is then deposited, by chemical vapor deposition, on the layer of alkali-inert inorganic material. A relatively thin polysilicon layer is then deposited at a temperature of 520 to 570 ° C on the layer of silicon oxide. This thin polysilicon layer is then annealed at a temperature of less than 650 ° C (preferably at a temperature of 580 - 620 ° C) in a nitrogen atmosphere.

Selected portions of this polysilicon layer are then removed by etching so as to form desired islands in this polysilicon layer and exposing selected areas of the silicon oxide layer. A thin gate oxide layer is then formed on these islands by oxidizing this island under a high pressure at a temperature below 650 ° C. Preferably a temperature range of 550 ° C - 650 ° C and a pressure of 5-50 atmospheres is employed. A gate is then formed on the gate oxide layer by depositing a heavily doped polysilicon layer on the gate oxide layer and etching portions of this relatively heavily doped polysilicon layers to form the gates. The p or n dopants are implanted in areas of the islands of polysilicon slightly adjacent to the gates to form lightly doped source and drain areas.

A thin layer of silicon oxide, preferably 500 Å - 50000 Å is then provided on the gate and on the adjacent doped source and drain areas by chemical vapor deposition. The layers of silicon adjacent to the relatively lightly doped source and drain areas are then heavily implanted with p or n dopants and annealed at a temperature below 650 ° C.

The resultant device is then hydrogenated at a temperature of less than about 450 ° C with a hydrogen plasma. Preferably, hydrogenation is carried out at a temperature of 200 ° C - 450 ° C.

The relatively lightly doped source and drain areas may be provided with an implant dose of 0 to 5 x 10^{13} atoms/cm^2 while the relatively heavily doped source and drain areas may be provided with an implant dose of 5 x 10^{13} - 5 x 10^{15} atoms/cm^2. The doping concentration in the heavily doped gate may be from 10^{19} to 10^{21} atoms/cm^3.

As a dopant, source BF_2 may be employed; however, other possible doping sources such as B, P, as may also be employed. Doping may be carried out by ion implantation.

Preferably, the relatively thick layer of silicon oxide has a thickness of 15,000 - 25,000 Å, the relatively thin polysilicon layer has a thickness of 800 - 1700 Å and the relatively thin layer of silicon oxide has a thickness of about 800 - 1200 Å. Preferably, the relatively thick polysilicon layer has a thickness of 4000 Å - 7000 Å.

When the substrate is relatively free of alkali, such as quartz or a semiconductor, the layer of the alkali-inert inorganic material and the relatively thick silicon oxide layer may be omitted. the relatively thin polysilicon layer may then be deposited directly on the substrate.

Example 1

On a cleaned glass wafer 1 a silicon nitride layer 2 of a thickness of about 1500 Å was deposited by an LPCVD process. A first relatively thick layer of silicon oxide 3 of a thickness of 2 microns was then deposited by a LPCVD process on the layer of silicon nitride. A relatively thin layer of polysilicon 4 was then deposited by a LPCVD process on a relatively thick layer 3 of silicon oxide. This layer 4 of silicon had a thickness of about 1500 Å. The polysilicon layer 4 was then annealed in a nitrogen atmosphere at a temperatur of about 600 ° C for about 48 hours.

The polysilicon layer 4 was then etched according to a desired pattern to form islands 5 from the polysilicon layer while leaving exposed portions of the silicon oxide layer 3.

A thin gate oxide layer 6 of a thickness of about 1000 Å was then formed on an island 5. A relatively thick polysilicon layer 7 of a thickness of about 5000 Å was then deposited on the gate oxide layer 6. The relatively thick polysilicon layer 7 was th n h avily implanted with a boron difluoride implanter. The resulting

In the examples in the table, leakage values are in picoamps per micron of gate width. The source to drain voltage was 5 volts for all these examples. Th "offset" referred to in th table is from the point of minimum leakage.

Claims

1. A low temperature method of manufacturing a thin film transistor having a low leakage current, said method comprising:
   a) depositing a thin layer of an alkali-inert inorganic material on a glass substrate having an annealing point less than 650 • C,
   b) depositing a first relatively thick layer of silicon oxide on the layer of inorganic material by chemical vapor deposition,
   c) depositing a relatively thin amorphous silicon layer, at a temperature of 520-570 • C, on the first layer of silicon oxide,
   d) annealing said relatively thin amorphous silicon layer at a temperature of less than 650 • C in a nitrogen atmosphere, to form a large grain polysilicon layer,
   e) etching said relatively thin polysilicon layer to remove portions of said polysilicon layer and expose selected areas of said first layer of silicon oxide and form islands in said polysilicon layer,
   f) oxidizing at least one of said islands under high pressure at a temperature below 650 • C to form a thin gate oxide layer on said island(s) of polysilicon,
   g) depositing a relatively thick, heavily doped polysilicon layer on said gate oxide layer and etching away portions of said relatively heavily doped polysilicon layer to form a gate,
   h) relatively lightly implanting p or n dopants in areas of said island of polysilicon laterally adjacent to said gate to form lightly doped source and drain areas,
   i) providing by chemical vapor deposition a second relatively thin layer of silicon oxide on said gate and on adjacent lightly doped source and drain areas,
   j) relatively heavily doping areas of said first layer of silicon adjacent to said relatively lightly doped source and drain areas,
   k) annealing said source and drain areas at a temperature below 650 • C, and
   l) hydrogenating the resultant device at a temperature of 200-400 • C with a hydrogen plasma.

2. The method of Claim 1 wherein the alkali-inert inorganic material is silicon nitride.

3. The method of Claim 2 wherein the substrate has an annealing point of about 550-650 • C.

4. The method of Claim 3 wherein said relatively thick polysilicon layer is annealed at a temperature of 580-620 • C.

5. The method of Claim 4 wherein the gate oxide layer is formed by heating the island at 550-650 • C at a pressure of 5-50 atmospheres.

6. A method of manufacturing a thin film transistor exhibiting a reduced reverse leakage current, said method comprising:
   a) forming a first relatively thick layer of silicon oxide on a semiconductor substrate,
   b) depositing a relatively thin polysilicon layer at a temperature of less than 650 • C on said first layer of silicon oxide,
   c) annealing said relatively thin polysilicon layer in a nitrogen atmosphere,
   d) removing, by etching, selective portions of said relatively thin polysilicon layer to expose selective portions of said first layer of silicon oxide and forming islands in said relatively thin polysilicon layer,
   e) oxidizing at least one of said islands under high pressure at a temperature below about 650 • C to form a thin gate oxide layer on said island(s) of said relatively thin polysilicon layer,
   f) depositing a second relatively thick polysilicon layer on said gat oxide layer,
   g) heavily doping said second polysilicon layer and etching away, by reactive ion etching, portions of the resultant doped second polysilicon layer to form a gate,
   h) relatively lightly doping resultant exposed areas of said island of said layer of polysilicon laterally adjacent to said gate to form lightly doped source and drain ar as,
   i) providing a relatively thin, layer of silicon oxide on said gate and on said adjacent lightly doped

source and drain areas,
j) relatively heavily doping exposed areas of said island of said layer of polysilicon adjacent to said lightly dop d source and drain areas to form relatively heavily doped source and drain areas,
k) annealing said source and drain areas at a temperature of 600-750 ° C, and
l) hydrogenating the resultant device at a temperature of l ss than about 400 ° C with a hydrogen plasma.

7. The method of Claim 6 wherein said high pressure oxidation of said island is carried out at a temperature of 550 - 650 ° C under a pressure of 5 - 50 atmospheres.

8. The method of Claim 7 wherein the device is hydrogenated at 200 - 450 ° C.

9. The method of Claim 8 wherein the second polysilicon layer is doped with BF_3.

10. The method of Claim 8 wherein said first polysilicon layer has a thickness of about 500 Å to 1500 Å and said second polysilicon layer has a thickness of about 4000 Å to 7000 Å.

11. The method of Claim 1 wherein the first, relatively thick, layer of silicon oxide is deposited by chemical vapor deposition.

12. The method of Claim 2 wherein the first, relatively thick, layer of silicon oxide is deposited by chemical vapor deposition.

13. The method of Claim 5 wherein the thin layer of silicon nitride has a thickness of 800-1200Å and the relatively thick silicon oxide layer has a thickness of 17,000 - 23,000Å.

14. A thin film transistor exhibiting a low leakage current upon reverse biasing said transistor comprising
a) a glass substrate having an annealing point greater than 650 ° C,
b) a relatively thin layer of an alkali-inert inorganic material deposed on said substrate,
c) a first relatively thick layer of silicon oxide deposed on said alkali-inert inorganic material,
d) a first relatively thin polysilicon layer deposed on said first relatively thick layer of silicon oxide,
e) a relatively thin gate oxide deposed on said first relatively thin polysilicon layer,
f) a gate, provided by a relatively heavily doped area,
g) a second relatively thick polysilicon layer provided on a portion of the surface of said gate oxide layer,
h) relatively lightly doped source and drain areas provided in portions of said first relatively thin layer of polysilicon laterally adjacent to said gate,
i) a relatively thin silicon oxide layer provided on said gate and on said lightly doped source and drain areas,
j) relatively heavily doped source and drain areas provided in portions of said first relatively thin layer of polysilicon laterally adjacent to said relatively slightly doped source and drain areas,
said source and drain areas being annealed.

15. The thin film transistor of Claim 14 wherein the alkali-inert inorganic material is silicon nitride.

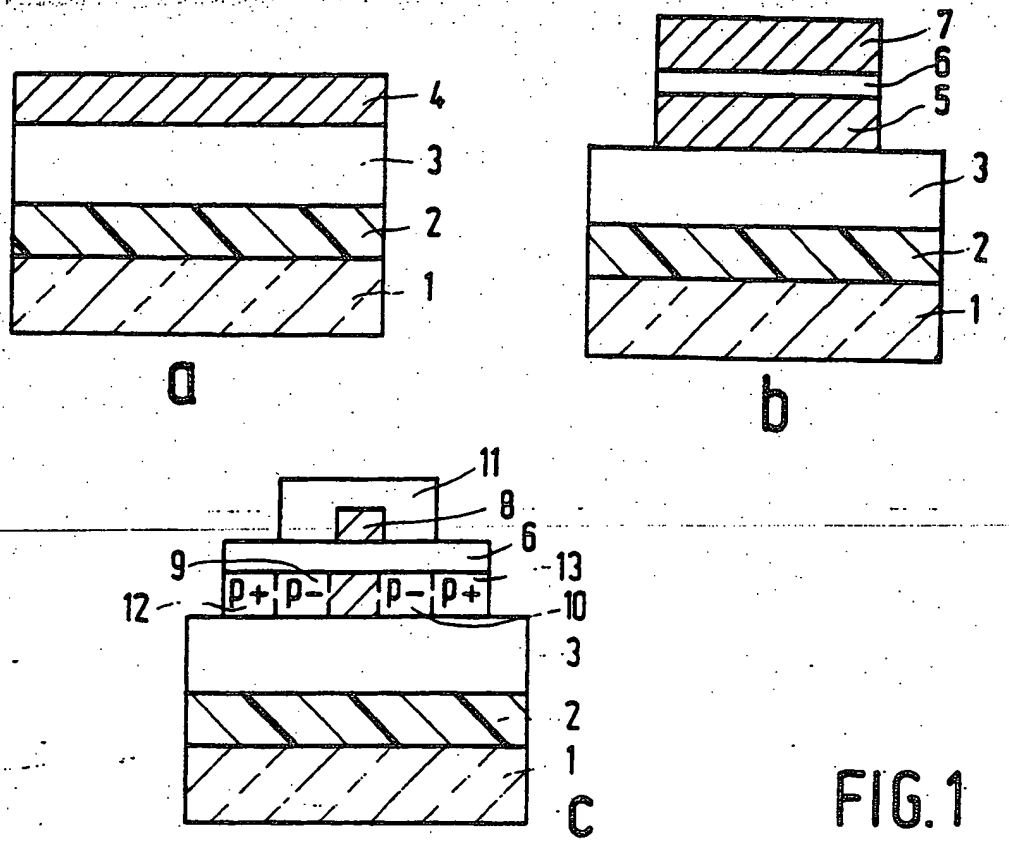
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FIG.1

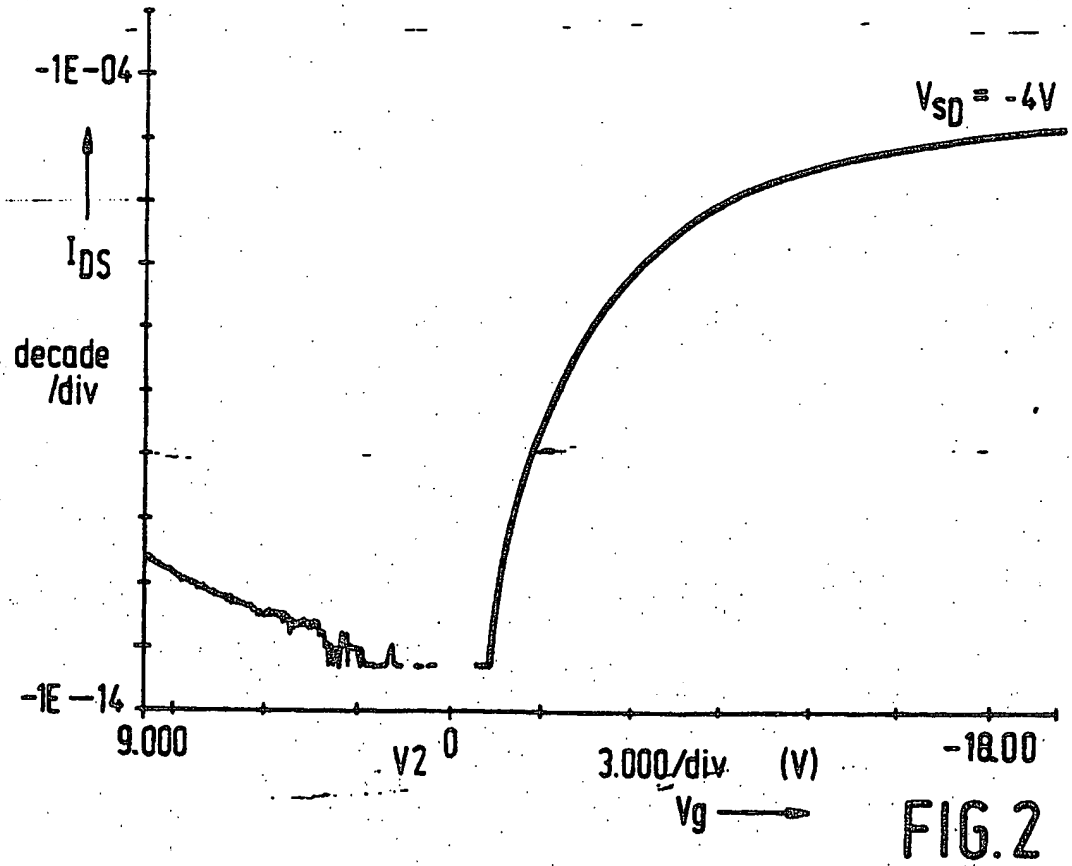
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FIG.2

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Application Number

EP 91 20 2178

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	IEEE TRANSACTIONS ON ELECTRON DEVICES. vol. 36, no. 9-I, September 1989, NEW YORK US pages 1929 - 1933; TADASHI SERIKAWA ET AL: 'Low-Temperature Fabrication of High-Mobility Poly-Si TFT,s for Large-Area LCD,s' * abstract; figure 1 * * paragraph 2 *	1,14	H01L29/784
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	07 JANUARY 1992	MIMOUN B.J.

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	IEEE ELECTRON DEVICE LETTERS. vol. EDL-8, no. 9, September 1987, NEW YORK US pages 425 - 427; SHUNJI SEKI ET AL: 'Laser-Recrystallized Polycrystalline-Silicon Thin-Film Transistors with Low Leakage Current and High Switching Ratio' * paragraph 2; figure 1 *	1,6	
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